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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
2133	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/816,165	Applicant(s) TAKEDA ET AL.	
	Examiner Dipakkumar Gandhi	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 March 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2, 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

- On page 11, lines 8-9, "$s = d_0C_0 \wedge d_1C_1 \wedge d_2C_2 \wedge d_3C_3 \wedge d_4C_4 \wedge d_5C_5 \wedge d_6C_6 \wedge d_7C_7 \wedge d_8C_8 \wedge d_9C_9$" is incorrect. It should be – $s = d_0C_0 \wedge d_1C_1 \wedge d_2C_2 \wedge d_3C_3 \wedge d_4C_4 \wedge d_5C_5 \wedge d_6M_1 \wedge d_7M_2 \wedge d_8M_3 \wedge d_9M_4$ --

.

- On page 14, lines 1-2, "$d_0C_0 \wedge d_1C_1 \wedge d_2C_2 \wedge d_3C_3 \wedge d_4C_4 \wedge d_5C_5 \wedge d_6C_6 \wedge d_7C_7 \wedge d_8C_8 \wedge d_9C_9 \wedge e$" is incorrect. It should be – $d_0C_0 \wedge d_1C_1 \wedge d_2C_2 \wedge d_3C_3 \wedge d_4C_4 \wedge d_5C_5 \wedge d_6M_1 \wedge d_7M_2 \wedge d_8M_3 \wedge d_9M_4 \wedge e$ --

.

- On page 21, line 12, "mask symbols" is incorrect. It should be –mask patterns--.
- On page 23, line 6, "checksum selector 46" is incorrect. It should be – checksum selector 44 — as per figure 3.
- On page 29, line 10, "multiplier 60 multiples" is incorrect. It should be -- multiplier 60 multiplies --.
- On page 32, line 27, "mask symbols" is incorrect. It should be – mask patterns --.
- On page 33, line 1, "symbols" is incorrect. It should be – patterns --.
- On page 34, line 8, "multiplier 22" is incorrect. It should be – multiplier 62 – as per figure 9.

Appropriate correction is required.

Drawings

2. The drawings are objected to because

- In figure 7, the connection from the top portion of item S82 to the arrow between item S62 and S64 is incorrect. The top portion of item S82 should be connected to the arrow between item S60 and item S62 as per page 32, lines 5-9 of the specification.
- In figure 10, the connection from the top portion of item S82 to the arrow between item S62 and S64 is incorrect. The top portion of item S82 should be connected to the arrow between item S60 and item S62 as per page 36, lines 10-16 of the specification.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-3, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over TSG-RAN Working Group 1 Meeting #6 (Harmonization Impact on TFCI and New Optimal Coding for extended TFCI with almost no Complexity Increase (rev 1), pp 1-12, July 13, 1999) in view of Chaib et al. (US 5,870,414) and Tokiwa et al. (New Decoding Algorithm for Reed-Muller Codes, IEEE Transactions on Information Theory, Vol. IT-28, No. 5, September 1982).

As per claim 1, TSG-RAN Working Group 1 Meeting #6 teaches an apparatus for decoding Reed-Muller code in which information data is encoded by using mask symbols and orthogonal codes and a Reed-Muller encoder configured to Reed-Muller encode the second portion of the information data output from the first decoder and the second decoder and the first portion of the information data (figure 4, 5, 13, pages 3, 4, 5, 11, 12, TSG-RAN Working Group 1 Meeting #6).

However TSG-RAN Working Group 1 Meeting #6 does not explicitly teach the specific use of the information data including a first portion and a second portion.

Chaib et al. in an analogous art teach according to a fourth aspect of the invention, there is provided apparatus for encoding a digital signal comprising a sequence of digital words, each comprising a first portion and a second portion, to provide a corresponding sequence of codewords, supplying the

sequence of codewords to a transmission or storage medium, extracting a corresponding sequence of codeword vectors from the transmission or storage medium, and decoding the sequence of codeword vectors to extract the originally-encoded sequence of digital words (col. 3, lines 37-46, Chaib et al.). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Chaib et al. by including an additional step of using the information data including a first portion and a second portion. This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the information data including a first portion and a second portion would provide the opportunity to improve reliability and bit error rates for a given signal-to-noise ratio for encoding/decoding digital signals for transmission.

TSG-RAN Working Group 1 Meeting #6 also does not explicitly teach the specific use of the apparatus comprising: an arithmetic operation unit configured to calculate a first exclusive OR of the Reed-Muller code and an exclusive ORed value of a candidate pattern of the mask symbols and the information data corresponding to the candidate pattern; a first decoder configured to calculate a checksum of the first exclusive OR and majority-decide the checksum to decode a part of the second portion of the information data corresponding to the orthogonal codes; a second decoder configured to calculate a second exclusive OR of the first exclusive OR and a product of the part of the second portion of the information data and the orthogonal codes and majority-decide the second exclusive OR to decode a remaining part of the second portion of the information data corresponding to the orthogonal codes; a minimum distance detector configured to detect the minimum of a Euclidean distance between an output from the Reed-Muller encoder and the Reed-Muller code supplied to the arithmetic operation unit while a plurality of candidate patterns of the mask symbols are supplied to the arithmetic operation unit, whereby the first portion of the information data is decoded based on the mask symbols corresponding to the minimum of the Euclidean distance.

However Tokiwa et al. in an analogous art teach that finite geometry codes including Euclidean geometry projective codes can be decoded with a majority-logic decoding algorithm (page 780, Tokiwa et al.). Tokiwa et al. also teach to apply the decoding algorithm for the 2^v-SI code on the basis of the code with

the minimum distance 2^{m-r-v} (page 783, Tokiwa et al.). Tokiwa et al. teach decoding Algorithm for Reed-Muller codes (page 783-785, Tokiwa et al.) and Decoding Complexity (page 785-786, Tokiwa et al.). The examiner would like to point out that $\oplus$ is an exclusive OR operation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Tokiwa et al. by including an additional step of using the apparatus comprising: an arithmetic operation unit configured to calculate a first exclusive OR of the Reed-Muller code and an exclusive ORed value of a candidate pattern of the mask symbols and the information data corresponding to the candidate pattern; a first decoder configured to calculate a checksum of the first exclusive OR and majority-decide the checksum to decode a part of the second portion of the information data corresponding to the orthogonal codes; a second decoder configured to calculate a second exclusive OR of the first exclusive OR and a product of the part of the second portion of the information data and the orthogonal codes and majority-decide the second exclusive OR to decode a remaining part of the second portion of the information data corresponding to the orthogonal codes; a minimum distance detector configured to detect the minimum of a Euclidean distance between an output from the Reed-Muller encoder and the Reed-Muller code supplied to the arithmetic operation unit while a plurality of candidate patterns of the mask symbols are supplied to the arithmetic operation unit, whereby the first portion of the information data is decoded based on the mask symbols corresponding to the minimum of the Euclidean distance.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that calculating a first exclusive OR of the Reed-Muller code and an exclusive ORed value of a candidate pattern of the mask symbols and the information data corresponding to the candidate pattern would provide the opportunity to exclude the mask pattern from the Reed-Muller code. It is easy to majority decide the Reed-Muller code excluding the mask pattern. Using a majority-logic decoding algorithm and a minimum distance detector, the decoding delay can be shortened.

- As per claim 2, TSG-RAN Working Group 1 Meeting #6, Chaib et al. and Tokiwa et al. teach the additional limitations.

Tokiwa et al. teach the apparatus further comprising a memory configured to store a plurality of exclusive ORed value of a plurality of candidate patterns of the mask symbols and a plurality of information data corresponding to the candidate patterns, and wherein the arithmetic operation unit calculates the first exclusive OR of the Reed-Muller codes and each of the plurality of exclusive ORed values stored in the memory (page 783, Tokiwa et al.). The examiner would like to point out that it is obvious to one of ordinary skill in the art to use memory to store data.

- As per claim 3, TSG-RAN Working Group 1 Meeting #6, Chaib et al. and Tokiwa et al. teach the additional limitations.

Chaib et al. teach the apparatus further comprising a hard decision unit configured to hard-decide the Reed-Muller code supplied to the arithmetic operation unit (col. 11, lines 3-6, Chaib et al.).

- As per claim 5, TSG-RAN Working Group 1 Meeting #6, Chaib et al. and Tokiwa et al. teach the additional limitations.

Claim 5 (method) follows the same limitations as claim 1 (apparatus). See rejection to claim 1, above. Claim 5 is rejected under the same rational as to claim 1 rejected above.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over TSG-RAN Working Group 1 Meeting #6 (Harmonization Impact on TFCI and New Optimal Coding for extended TFCI with almost no Complexity Increase (rev 1), pp 1-12, July 13, 1999), Chaib et al. (US 5,870,414) and Tokiwa et al. (New Decoding Algorithm for Reed-Muller Codes, IEEE Transactions on Information Theory, Vol. IT-28, No. 5, September 1982) as applied to claim 1 above, and further in view of Dapper et al. (US 6,282,683 B1).

As per claim 4, TSG-RAN Working Group 1 Meeting #6, Chaib et al. and Tokiwa et al. substantially teach the claimed invention described in claim 1 (as rejected above). Chaib et al. teach a hard decision unit configured to hard-decide an output from the accumulator (col. 11, lines 3-6, Chaib et al.).

However, TSG-RAN Working Group 1 Meeting #6, Chaib et al. and Tokiwa et al. do not explicitly teach the specific use of a memory configured to store the first exclusive OR output from the arithmetic operation unit; a checksum calculator configured to read bit data from the memory and calculate a plurality of exclusive ORs of a plurality of sets of the read bit data to obtain a plurality of checksums; a

selector configured to select some of the plurality of checksums based on a type of the Reed-Muller code; an accumulator configured to accumulate the selected checksums.

Dapper et al. in an analogous art teach that there are several types of memory 582 on the LANU 580. The first and largest is 8 MBytes of page-mode DRAM for the storage of LANU operational code (figure 103, col. 98, lines 11-13, Dapper et al.). Dapper et al. teach cyclical redundancy checksum (col. 59, line 59, Dapper et al.). Dapper et al. teach calculator 2630 (figure 74, col. 86, line 38, Dapper et al.). Dapper et al. teach accumulator 2633 (figure 74, col. 88, line 62, Dapper et al.) and selector 2643 (figure 74, col. 88, line 65, Dapper et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Dapper et al. by including an additional step of using a memory configured to store the first exclusive OR output from the arithmetic operation unit; a checksum calculator configured to read bit data from the memory and calculate a plurality of exclusive ORs of a plurality of sets of the read bit data to obtain a plurality of checksums; a selector configured to select some of the plurality of checksums based on a type of the Reed-Muller code; an accumulator configured to accumulate the selected checksums.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to decode the received digital signal and correct the transmission errors.

7. Claims 6-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over TSG-RAN Working Group 1 Meeting #6 (Harmonization Impact on TFCI and New Optimal Coding for extended TFCI with almost no Complexity Increase (rev 1), pp 1-12, July 13, 1999) in view of Chaib et al. (US 5,870,414), Tokiwa et al. (New Decoding Algorithm for Reed-Muller Codes, IEEE Transactions on Information Theory, Vol. IT-28, No. 5, September 1982) and Zook (US 6,662,336 B1).

As per claim 6, TSG-RAN Working Group 1 Meeting #6 teaches an apparatus for decoding Reed-Muller code in which information data is encoded by using mask symbols and orthogonal codes (figure 4, 5, 13, pages 3, 4, 5, 11, 12, TSG-RAN Working Group 1 Meeting #6).

However TSG-RAN Working Group 1 Meeting #6 does not explicitly teach the specific use of the information data including a first portion and a second portion.

Chaib et al. in an analogous art teach according to a fourth aspect of the invention, there is provided apparatus for encoding a digital signal comprising a sequence of digital words, each comprising a first portion and a second portion, to provide a corresponding sequence of codewords, supplying the sequence of codewords to a transmission or storage medium, extracting a corresponding sequence of codeword vectors from the transmission or storage medium, and decoding the sequence of codeword vectors to extract the originally-encoded sequence of digital words (col. 3, lines 37-46, Chaib et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Chaib et al. by including an additional step of using the information data including a first portion and a second portion.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the information data including a first portion and a second portion would provide the opportunity to improve reliability and bit error rates for a given signal-to-noise ratio for encoding/decoding digital signals for transmission.

TSG-RAN Working Group 1 Meeting #6 also does not explicitly teach the specific use of the apparatus comprising: a first arithmetic operation unit configured to calculate an exclusive OR of the Reed-Muller code and an exclusive ORed value of a candidate pattern of the mask symbols and the information data corresponding to the candidate pattern; a decoder configured to calculate a checksum of the exclusive OR and majority-decide the checksum to decode a part of the second portion of the information data corresponding to the orthogonal codes; a second arithmetic operation unit configured to calculate a first accumulation result of each bit of a product of an output from the decoder and the orthogonal codes and a second accumulation result of each bit of a product of the output from the decoder and the orthogonal codes and detect one of the first accumulation result and the second accumulation result which corresponds to a smaller Euclidean distance between the Reed-Muller code input to the first arithmetic operation unit and encoded data of decoded data; a minimum detector configured to detect the minimum of an output from the second arithmetic operation unit while a plurality of candidate patterns of the mask

symbols are supplied to the first arithmetic operation unit, whereby the first portion of the information data is decoded based on the mask symbols corresponding to the minimum of the output from the second arithmetic operation unit.

However Tokiwa et al. in an analogous art teach that finite geometry codes including Euclidean geometry projective codes can be decoded with a majority-logic decoding algorithm (page 780, Tokiwa et al.). Tokiwa et al. also teach to apply the decoding algorithm for the 2^v-SI code on the basis of the code with the minimum distance 2^{m-r-v} (page 783, Tokiwa et al.). Tokiwa et al. teach decoding Algorithm for Reed-Muller codes (page 783-785, Tokiwa et al.) and Decoding Complexity (page 785-786, Tokiwa et al.). The examiner would like to point out that $\oplus$ is an exclusive OR operation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Tokiwa et al. by including an additional step of using the apparatus comprising:: a first arithmetic operation unit configured to calculate an exclusive OR of the Reed-Muller code and an exclusive ORed value of a candidate pattern of the mask symbols and the information data corresponding to the candidate pattern; a decoder configured to calculate a checksum of the exclusive OR and majority-decide the checksum to decode a part of the second portion of the information data corresponding to the orthogonal codes; a second arithmetic operation unit configured to calculate a first accumulation result of each bit of a product of an output from the decoder and the orthogonal codes and a second accumulation result of each bit of a product of the output from the decoder and the orthogonal codes and detect one of the first accumulation result and the second accumulation result which corresponds to a smaller Euclidean distance between the Reed-Muller code input to the first arithmetic operation unit and encoded data of decoded data; a minimum detector configured to detect the minimum of an output from the second arithmetic operation unit while a plurality of candidate patterns of the mask symbols are supplied to the first arithmetic operation unit, whereby the first portion of the information data is decoded based on the mask symbols corresponding to the minimum of the output from the second arithmetic operation unit.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that calculating an exclusive

OR of the Reed-Muller code and an exclusive ORed value of a candidate pattern of the mask symbols and the information data corresponding to the candidate pattern would provide the opportunity to exclude the mask pattern from the Reed-Muller code. It is easy to majority decide the Reed-Muller code excluding the mask pattern. Using a majority-logic decoding algorithm and a minimum distance detector, the decoding delay can be shortened.

TSG-RAN Working Group 1 Meeting #6 also does not explicitly teach the specific use of the inverted bit. However Zook in an analogous art teaches an inverse generator 104 (figure 2, col. 9, line 47, Zook). The inverse generator 104 (shown in detail in FIG. 5) comprises two inverse look up tables. The output of inverse look up table is four serial bits (figure 5, col. 14, lines 28-29, lines 38-39, Zook).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Zook by including an additional step of using the inverted bit.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the inverted bit would provide the opportunity to perform a bit order transformation for the quantity including the inverse of the prior discrepancy.

- As per claim 7, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Tokiwa et al. and Zook teach the additional limitations.

Tokiwa et al. teach the apparatus further comprising a memory configured to store a plurality of exclusive ORed value of a plurality of candidate patterns of the mask symbols and a plurality of information data corresponding to the candidate patterns, and wherein the first arithmetic operation unit calculates the exclusive OR of the Reed-Muller codes and each of the plurality of exclusive ORed values stored in the memory (page 783, Tokiwa et al.). The examiner would like to point out that it is obvious to one of ordinary skill in the art to use memory to store data.

- As per claim 8, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Tokiwa et al. and Zook teach the additional limitations.

Chaib et al. teach the apparatus further comprising a hard decision unit configured to hard-decide the Reed-Muller code supplied to the first arithmetic operation unit (col. 11, lines 3-6, Chaib et al.).

- As per claim 10, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Tokiwa et al. and Zook teach the additional limitations.

Claim 10 (method) follows the same limitations as claim 6 (apparatus). See rejection to claim 6, above. Claim 10 is rejected under the same rational as to claim 6 rejected above.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over TSG-RAN Working Group 1 Meeting #6 (Harmonization Impact on TFCI and New Optimal Coding for extended TFCI with almost no Complexity Increase (rev 1), pp 1-12, July 13, 1999), Chaib et al. (US 5,870,414), Tokiwa et al. (New Decoding Algorithm for Reed-Muller Codes, IEEE Transactions on Information Theory, Vol. IT-28, No. 5, September 1982) and Zook (US 6,662,336 B1) as applied to claim 6 above, and further in view of Dapper et al. (US 6,282,683 B1).

As per claim 9, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Tokiwa et al. and Zook substantially teach the claimed invention described in claim 6 (as rejected above). Chaib et al. teach a hard decision unit configured to hard-decide an output from the accumulator (col. 11, lines 3-6, Chaib et al.). However, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Tokiwa et al. and Zook do not explicitly teach the specific use of a memory configured to store the exclusive OR output from the arithmetic operation unit; a checksum calculator configured to read bit data from the memory and calculate a plurality of exclusive ORs of a plurality of sets of the read bit data to obtain a plurality of checksums; a selector configured to select some of the plurality of checksums based on a type of the Reed-Muller code; an accumulator configured to accumulate the selected checksums.

However Dapper et al. in an analogous art teach that there are several types of memory 582 on the LANU 580. The first and largest is 8 MBytes of page-mode DRAM for the storage of LANU operational code (figure 103, col. 98, lines 11-13, Dapper et al.). Dapper et al. teach cyclical redundancy checksum (col. 59, line 59, Dapper et al.). Dapper et al. teach calculator 2630 (figure 74, col. 86, line 38, Dapper et al.). Dapper et al. teach accumulator 2633 (figure 74, col. 88, line 62, Dapper et al.) and selector 2643 (figure 74, col. 88, line 65, Dapper et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Dapper et al. by including an additional step of using a memory configured to store the exclusive OR output from the arithmetic operation unit; a checksum calculator configured to read bit data from the memory and calculate a plurality of exclusive ORs of a plurality of sets of the read bit data to obtain a plurality of checksums; a selector configured to select some of the plurality of checksums based on a type of the Reed-Muller code; an accumulator configured to accumulate the selected checksums.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to decode the received digital signal and correct the transmission errors.

9. Claims 11-12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over TSG-RAN Working Group 1 Meeting #6 (Harmonization Impact on TFCI and New Optimal Coding for extended TFCI with almost no Complexity Increase (rev 1), pp 1-12, July 13, 1999) in view of Chaib et al. (US 5,870,414), Pyndiah et al. (US 6,065,147), Tokiwa et al. (New Decoding Algorithm for Reed-Muller Codes, IEEE Transactions on Information Theory, Vol. IT-28, No. 5, September 1982) and Dohi et al. (US 5,638,362).

As per claim 11, TSG-RAN Working Group 1 Meeting #6 teaches an apparatus for decoding Reed-Muller code in which information data is encoded by using mask symbols and orthogonal codes; a Reed-Muller encoder configured to Reed-Muller encode the second portion of the information data output from the first decoder and the second decoder and the first portion of the information data (figure 4, 5, 13, pages 3, 4, 5, 11, 12, TSG-RAN Working Group 1 Meeting #6).

However TSG-RAN Working Group 1 Meeting #6 does not explicitly teach the specific use of the information data including a first portion and a second portion.

Chaib et al. in an analogous art teach according to a fourth aspect of the invention, there is provided apparatus for encoding a digital signal comprising a sequence of digital words, each comprising a first portion and a second portion, to provide a corresponding sequence of codewords, supplying the sequence of codewords to a transmission or storage medium, extracting a corresponding sequence of

codeword vectors from the transmission or storage medium, and decoding the sequence of codeword vectors to extract the originally-encoded sequence of digital words (col. 3, lines 37-46, Chaib et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Chaib et al. by including an additional step of using the information data including a first portion and a second portion.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the information data including a first portion and a second portion would provide the opportunity to improve reliability and bit error rates for a given signal-to-noise ratio for encoding/decoding digital signals for transmission.

TSG-RAN Working Group 1 Meeting #6 also does not explicitly teach the specific use of the product of two codes.

However Pyndiah et al. in an analogous art teach the block code applied by the channel coder 12 is a product code obtained from systematic elementary codes. In the embodiment described below, it is the product of two linear block codes C_1, C_2 with respective parameters (n_1,k_1,d_1) and (n_2,k_2,d_2), (figure 1, col. 8, lines 19-23, Pyndiah et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Pyndiah et al. by including an additional step of using the product of two codes.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the product of the codes would provide the opportunity to enhance the performances of error-correcting codes by using concatenation techniques.

TSG-RAN Working Group 1 Meeting #6 also does not explicitly teach the specific use of the apparatus comprising: an arithmetic operation unit configured to calculate a first product of the Reed-Muller code and an exclusive ORed value of a candidate pattern of the mask symbols and the information data corresponding to the candidate pattern; a first decoder configured to calculate a checksum of the first product and majority-decide the checksum to decode a part of the second portion of the information data

corresponding to the orthogonal codes; a second decoder configured to calculate a second product of the first product and a product of the part of the second portion of the information data and the orthogonal codes and majority-decides the second product to decode a remaining part of the second portion of the information data corresponding to the orthogonal codes.

However Tokiwa et al. in an analogous art teach that finite geometry codes including Euclidean geometry projective codes can be decoded with a majority-logic decoding algorithm (page 780, Tokiwa et al.). Tokiwa et al. also teach to apply the decoding algorithm for the 2^v-SI code on the basis of the code with the minimum distance 2^{m-r-v} (page 783, Tokiwa et al.). Tokiwa et al. teach decoding Algorithm for Reed-Muller codes (page 783-785, Tokiwa et al.) and Decoding Complexity (page 785-786, Tokiwa et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Tokiwa et al. by including an additional step of using the apparatus comprising: an arithmetic operation unit configured to calculate a first product of the Reed-Muller code and an exclusive ORed value of a candidate pattern of the mask symbols and the information data corresponding to the candidate pattern; a first decoder configured to calculate a checksum of the first product and majority-decide the checksum to decode a part of the second portion of the information data corresponding to the orthogonal codes; a second decoder configured to calculate a second product of the first product and a product of the part of the second portion of the information data and the orthogonal codes and majority-decides the second product to decode a remaining part of the second portion of the information data corresponding to the orthogonal codes.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a majority-logic decoding algorithm would provide the opportunity to shorten the decoding delay.

TSG-RAN Working Group 1 Meeting #6 also does not explicitly teach the specific use of the apparatus comprising: a maximum correlation detector configured to detect the maximum of a correlation between an output from the Reed-Muller encoder and the Reed-Muller code supplied to the arithmetic operation unit while a plurality of candidate patterns of the mask symbols are supplied to the arithmetic operation

unit, whereby the first portion of the information data is decoded based on the mask symbols corresponding to the maximum of the correlation.

Dohi et al. in an analogous art teach that FIG. 7 is a block diagram of a correlation detector of a second embodiment (figure 7, col. 12, lines 35-36, Dohi et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Dohi et al. by including an additional step of using the apparatus comprising: a maximum correlation detector configured to detect the maximum of a correlation between an output from the Reed-Muller encoder and the Reed-Muller code supplied to the arithmetic operation unit while a plurality of candidate patterns of the mask symbols are supplied to the arithmetic operation unit, whereby the first portion of the information data is decoded based on the mask symbols corresponding to the maximum of the correlation.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a maximum correlation detector would provide the opportunity to determine the correct information data bits as a part of decoding process when the maximum correlation is detected between the received coded signal and the output from the Reed-Muller encoder.

- As per claim 12, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Pyndiah et al., Tokiwa et al. and Dohi et al. teach the additional limitations.

Tokiwa et al. teach the apparatus further comprising a memory configured to store a plurality of exclusive ORed value of a plurality of candidate patterns of the mask symbols and a plurality of information data corresponding to the candidate patterns, and wherein the arithmetic operation unit calculates the first product of the Reed-Muller codes and each of the plurality of exclusive ORed values stored in the memory (page 783, Tokiwa et al.).

Pyndiah et al. teach product of two codes (figure 1, col. 8, lines 19-23, Pyndiah et al.).

The examiner would like to point out that it is obvious to one of ordinary skill in the art to use memory to store data.

- As per claim 14, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Pyndiah et al., Tokiwa et al. and Dohi et al. teach the additional limitations.

Claim 14 (method) follows the same limitations as claim 11 (apparatus). See rejection to claim 11, above. Claim 14 is rejected under the same rational as to claim 11 rejected above.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over TSG-RAN Working Group 1 Meeting #6 (Harmonization Impact on TFCI and New Optimal Coding for extended TFCI with almost no Complexity Increase (rev 1), pp 1-12, July 13, 1999), Chaib et al. (US 5,870,414), Pyndiah et al. (US 6,065,147), Tokiwa et al. (New Decoding Algorithm for Reed-Muller Codes, IEEE Transactions on Information Theory, Vol. IT-28, No. 5, September 1982) and Dohi et al. (US 5,638,362) as applied to claim 11 above, and further in view of Dapper et al. (US 6,282,683 B1).

As per claim 13, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Pyndiah et al., Tokiwa et al. and Dohi et al. substantially teach the claimed invention described in claim 11 (as rejected above). Pyndiah et al. also teach product of two codes (figure 1, col. 8, lines 19-23, Pyndiah et al.).

However, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Pyndiah et al., Tokiwa et al. and Dohi et al. do not explicitly teach the specific use of a memory configured to store the first product; a checksum calculator configured to read bit data from the memory and calculate a plurality of exclusive ORs of a plurality of sets of the read bit data to obtain a plurality of checksums; a selector configured to select some of the plurality of checksums based on a type of the Reed-Muller code; an accumulator configured to accumulate the selected checksums.

Dapper et al. in an analogous art teach that there are several types of memory 582 on the LANU 580. The first and largest is 8 MBytes of page-mode DRAM for the storage of LANU operational code (figure 103, col. 98, lines 11-13, Dapper et al.). Dapper et al. teach cyclical redundancy checksum (col. 59, line 59, Dapper et al.). Dapper et al. teach calculator 2630 (figure 74, col. 86, line 38, Dapper et al.). Dapper et al. teach accumulator 2633 (figure 74, col. 88, line 62, Dapper et al.) and selector 2643 (figure 74, col. 88, line 65, Dapper et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Dapper et al. by

including an additional step of using a memory configured to store the first product; a checksum calculator configured to read bit data from the memory and calculate a plurality of exclusive ORs of a plurality of sets of the read bit data to obtain a plurality of checksums; a selector configured to select some of the plurality of checksums based on a type of the Reed-Muller code; an accumulator configured to accumulate the selected checksums.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to decode the received digital signal and correct the transmission errors.

11. Claims 15-16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over TSG-RAN Working Group 1 Meeting #6 (Harmonization Impact on TFCI and New Optimal Coding for extended TFCI with almost no Complexity Increase (rev 1), pp 1-12, July 13, 1999) in view of Chaib et al. (US 5,870,414), Pyndiah et al. (US 6,065,147), Tokiwa et al. (New Decoding Algorithm for Reed-Muller Codes, IEEE Transactions on Information Theory, Vol. IT-28, No. 5, September 1982), Zook (US 6,662,336 B1) and Jin (US 6,658,045 B1).

As per claim 15, TSG-RAN Working Group 1 Meeting #6 teaches an apparatus for decoding Reed-Muller code in which information data is encoded by using mask symbols and orthogonal codes (figure 4, 5, 13, pages 3, 4, 5, 11, 12, TSG-RAN Working Group 1 Meeting #6).

However TSG-RAN Working Group 1 Meeting #6 does not explicitly teach the specific use of the information data including a first portion and a second portion.

Chaib et al. in an analogous art teach according to a fourth aspect of the invention, there is provided apparatus for encoding a digital signal comprising a sequence of digital words, each comprising a first portion and a second portion, to provide a corresponding sequence of codewords, supplying the sequence of codewords to a transmission or storage medium, extracting a corresponding sequence of codeword vectors from the transmission or storage medium, and decoding the sequence of codeword vectors to extract the originally-encoded sequence of digital words (col. 3, lines 37-46, Chaib et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Chaib et al. by including an additional step of using the information data including a first portion and a second portion. This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the information data including a first portion and a second portion would provide the opportunity to improve reliability and bit error rates for a given signal-to-noise ratio for encoding/decoding digital signals for transmission.

TSG-RAN Working Group 1 Meeting #6 also does not explicitly teach the specific use of the product of two codes.

However Pyndiah et al. in an analogous art teach the block code applied by the channel coder 12 is a product code obtained from systematic elementary codes. In the embodiment described below, it is the product of two linear block codes C_1, C_2 with respective parameters (n_1,k_1,d_1) and (n_2,k_2,d_2), (figure 1, col. 8, lines 19-23, Pyndiah et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Pyndiah et al. by including an additional step of using the product of two codes.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the product of the codes would provide the opportunity to enhance the performances of error-correcting codes by using concatenation techniques.

TSG-RAN Working Group 1 Meeting #6 also does not explicitly teach the specific use of the apparatus comprising: a first arithmetic operation unit configured to calculate a first product of the Reed-Muller code and an exclusive ORed value of a candidate pattern of the mask symbols and the information data corresponding to the candidate pattern; a decoder configured to calculate a checksum of the first product and majority-decide the checksum to decode a part of the second portion of the information data corresponding to the orthogonal codes; a second arithmetic operation unit configured to calculate a first accumulation result of each bit of a product of an output from the decoder and the orthogonal codes and

a second accumulation result of each bit of a product of the output from the decoder and the orthogonal codes and detect a larger one of the first accumulation result and the second accumulation result. A plurality of candidate patterns of the mask symbols are supplied to the first arithmetic operation unit, whereby the first portion of the information data is decoded based on the mask symbols.

However Tokiwa et al. in an analogous art teach that finite geometry codes including Euclidean geometry projective codes can be decoded with a majority-logic decoding algorithm (page 780, Tokiwa et al.). Tokiwa et al. also teach to apply the decoding algorithm for the 2^v-SI code on the basis of the code with the minimum distance 2^{m-r-v} (page 783, Tokiwa et al.). Tokiwa et al. teach decoding Algorithm for Reed-Muller codes (page 783-785, Tokiwa et al.) and Decoding Complexity (page 785-786, Tokiwa et al.). The examiner would like to point out that $\oplus$ is an exclusive OR operation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Tokiwa et al. by including an additional step of using the apparatus comprising: a first arithmetic operation unit configured to calculate a first product of the Reed-Muller code and an exclusive ORed value of a candidate pattern of the mask symbols and the information data corresponding to the candidate pattern; a decoder configured to calculate a checksum of the first product and majority-decide the checksum to decode a part of the second portion of the information data corresponding to the orthogonal codes; a second arithmetic operation unit configured to calculate a first accumulation result of each bit of a product of an output from the decoder and the orthogonal codes and a second accumulation result of each bit of a product of the output from the decoder and the orthogonal codes and detect a larger one of the first accumulation result and the second accumulation result. A plurality of candidate patterns of the mask symbols are supplied to the first arithmetic operation unit, whereby the first portion of the information data is decoded based on the mask symbols.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a majority-logic decoding algorithm the decoding delay could be shortened.

TSG-RAN Working Group 1 Meeting #6 also does not explicitly teach the specific use of the inverted bit.

However Zook in an analogous art teaches an inverse generator 104 (figure 2, col. 9, line 47, Zook). The inverse generator 104 (shown in detail in FIG. 5) comprises two inverse look up tables. The output of inverse look up table is four serial bits (figure 5, col. 14, lines 28-29, lines 38-39, Zook).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Zook by including an additional step of using the inverted bit.
This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the inverted bit would provide the opportunity to perform a bit order transformation for the quantity including the inverse of the prior discrepancy.
TSG-RAN Working Group 1 Meeting #6 also does not explicitly teach the specific use of the maximum detector configured to detect the maximum of an output from the second arithmetic operation unit and data is decoded corresponding to the maximum of the output from the second arithmetic operation unit.
However Jin in an analogous art teaches that at the maximum detector 460, the largest element in the composite vector 458 is selected and output to the low-pass filters (figure 4B, col. 17, lines 36-38, Jin).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Jin by including an additional step of using the maximum detector configured to detect the maximum of an output from the second arithmetic operation unit and data is decoded corresponding to the maximum of the output from the second arithmetic operation unit.
This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using maximum detector would provide the opportunity to decode the data using the maximum output value.

- As per claim 16, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Pyndiah et al., Tokiwa et al., Zook and Jin teach the additional limitations.

Tokiwa et al. teach the apparatus further comprising a memory configured to store a plurality of exclusive ORed value of a plurality of candidate patterns of the mask symbols and a plurality of information data

corresponding to the candidate patterns, and wherein the first arithmetic operation unit calculates the first product of the Reed-Muller codes and each of the plurality of exclusive ORed values stored in the memory (page 783, Tokiwa et al.).

Pyndiah et al. teach product of two codes (figure 1, col. 8, lines 19-23, Pyndiah et al.).

The examiner would like to point out that it is obvious to one of ordinary skill in the art to use memory to store data.

- As per claim 18, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Pyndiah et al., Tokiwa et al., Zook and Jin teach the additional limitations.

Claim 18 (method) follows the same limitations as claim 15 (apparatus). See rejection to claim 15, above. Claim 18 is rejected under the same rational as to claim 15 rejected above.

12. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over TSG-RAN Working Group 1 Meeting #6 (Harmonization Impact on TFCI and New Optimal Coding for extended TFCI with almost no Complexity Increase (rev 1), pp 1-12, July 13, 1999), Chaib et al. (US 5,870,414), Pyndiah et al. (US 6,065,147), Tokiwa et al. (New Decoding Algorithm for Reed-Muller Codes, IEEE Transactions on Information Theory, Vol. IT-28, No. 5, September 1982), Zook (US 6,662,336 B1) and Jin (US 6,658,045 B1) as applied to claim 15 above, and further in view of Dapper et al. (US 6,282,683 B1).

As per claim 17, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Pyndiah et al., Tokiwa et al., Zook and Jin substantially teach the claimed invention described in claim 15 (as rejected above). Pyndiah et al. also teach product of two codes (figure 1, col. 8, lines 19-23, Pyndiah et al.).

However, TSG-RAN Working Group 1 Meeting #6, Chaib et al., Pyndiah et al., Tokiwa et al., Zook and Jin do not explicitly teach the specific use of the apparatus wherein the decoder comprises: a memory configured to store the first product; a checksum calculator configured to read bit data from the memory and calculate a plurality of exclusive ORs of a plurality of sets of the read bit data to obtain a plurality of checksums; a selector configured to select some of the plurality of checksums based on a type of the Reed-Muller code; and an accumulator configured to accumulate the selected checksums.

Dapper et al. in an analogous art teach that there are several types of memory 582 on the LANU 580. The first and largest is 8 MBytes of page-mode DRAM for the storage of LANU operational code (figure

103, col. 98, lines 11-13, Dapper et al.). Dapper et al. teach cyclical redundancy checksum (col. 59, line 59, Dapper et al.). Dapper et al. teach calculator 2630 (figure 74, col. 86, line 38, Dapper et al.). Dapper et al. teach accumulator 2633 (figure 74, col. 88, line 62, Dapper et al.) and selector 2643 (figure 74, col. 88, line 65, Dapper et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify TSG-RAN Working Group 1 Meeting #6's document with the teachings of Dapper et al. by including an additional step of using the apparatus wherein the decoder comprises: a memory configured to store the first product; a checksum calculator configured to read bit data from the memory and calculate a plurality of exclusive ORs of a plurality of sets of the read bit data to obtain a plurality of checksums; a selector configured to select some of the plurality of checksums based on a type of the Reed-Muller code; and an accumulator configured to accumulate the selected checksums.

This modification would have been obvious to one of the ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to decode the received digital signal and correct the transmission errors.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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